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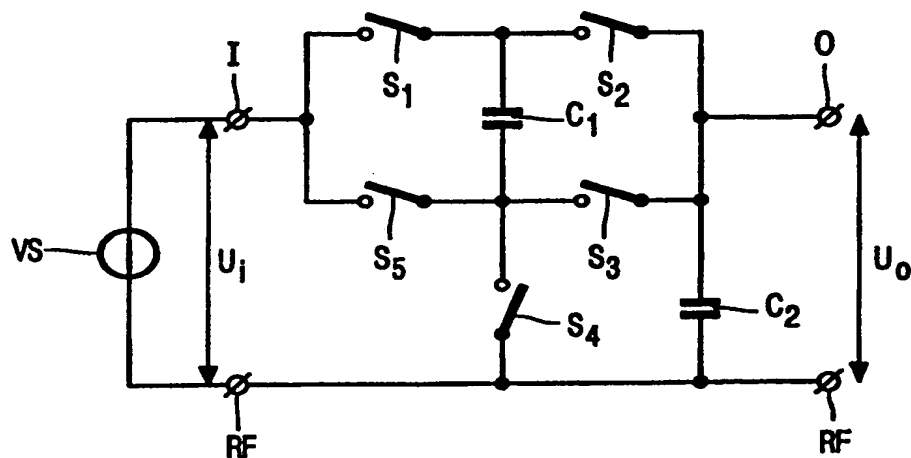
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amendments.

(54) Title: COMBINED CAPACITIVE UP/DOWN CONVERTER

(57) Abstract

A switched capacitive voltage converter for converting an input voltage (U_i) between an input terminal (I) and reference terminal (RF) to an output voltage (U_o) between an output terminal (O) and the reference terminal (RF). The voltage converter comprises only two capacitors (C_1 , C_2) and five switches (S_1 – S_5). The first (S_1) and the second switch (S_2) are coupled in series between the input terminal (I) and the output terminal (O). The third (S_3) and the fifth (S_5) switch are also coupled between the input terminal (I) and the output terminal (O). The first capacitor (C_1) is coupled in series between a node common to the first (S_1) and the second (S_2) switches and a node common to the third (S_3) and the fifth (S_5) switch. The fourth switch (S_4) is coupled between the node common to the third (S_3) and the fifth (S_5) switch and the reference terminal (RF). The second capacitor (C_2) is coupled between the output terminal (O) and the reference terminal (RF). The voltage converter disclosed herein can operate as an up converter, a down converter as well as a buffer.



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Combined capacitive up/down converter

The invention relates to a switched capacitive voltage converter for converting an input voltage between an input terminal and reference terminal to an output voltage between an output terminal and the reference terminal.

Switched capacitive voltage converters of the type defined in the opening
5 paragraph are known from the general state of the art. Switched capacitive voltage converters are used inter alia in battery-powered apparatuses, in which a high efficiency is important, because they make it possible to realize converters which have a high efficiency and which, in addition, generate low-level electromagnetic fields (also briefly referred to as EM fields), unlike converters which use a coil for the storage of energy.

10 For certain uses it is necessary to convert the input voltage to a higher output voltage. For these uses it is possible to employ, for example, switched capacitive voltage converters as described in European Patent Specification EP 0 461 717 A1. For other uses it is desirable to convert the input voltage to a lower output voltage. For the last-mentioned uses it is possible to employ, for example, switched capacitive voltage converters as described in
15 United States Patent Specification 4,389,704.

There are also uses, such as for example the so-called class G audio amplifiers, where it is desirable for reasons of efficiency that at a given instant the input voltage is converted to a higher output voltage and at another instant the input voltage is converted to a lower output voltage.

20 A drawback of the switched capacitive voltage converters as described in said European Patent Specifications is that they can operate solely as an up converter and a down converter, respectively, but not as a combined up/down converter.

Switched capacitive up/down converters are known from the general state of the art but these are made up of a separate opening converter and a separate down converter. A
25 drawback is that they require a comparatively large number of components. Particularly in the case of use in an integrated circuit (IC) it is important to minimize the number of capacitive elements because these elements occupy a comparatively large portion of the required chip area.

Another drawback of the afore-mentioned capacitive up/down converters in accordance with the generate state of the art is that they require a comparatively large number of IC pins for the connection of external components.

5 A further drawback of the afore-mentioned capacitive up/down converters in accordance with the general state of the art is that they dissipate comparatively much power.

It is an object of the invention to provide a combined capacitive up/down converter which does not have the afore-mentioned drawbacks.

To this end, according to the invention, the switched capacitive voltage converter of the type defined in the opening paragraph is characterized in that the switched capacitive voltage
10 converter comprises: a first capacitive element; a second capacitive element coupled between the output terminal and the reference terminal; first switching means coupled between the input terminal and a first electrode of the first capacitive element; second switching means coupled between the output terminal and the first electrode of the first capacitive element; third switching means coupled between the output terminal and a second electrode of the first
15 capacitive element; first switching means coupled between the first electrode of the first capacitive element and the reference terminal; and fifth switching means coupled between the input terminal and the second electrode of the first capacitive element. Thus, it is achieved in a simple manner that a switched capacitive voltage converter having only two capacitive elements and five switching means is obtained which at option operates in one of the
20 following three modes: up conversion, down conversion, or buffering, in which last-mentioned mode the output voltage is substantially equal to the input voltage. As, in contradistinction to the switched capacitive voltage converter in accordance with the general state of the art, the switched capacitive voltage converter in accordance with the invention always operates in only one of the three afore-mentioned modes the current consumption and, consequently, also
25 the dissipation is low. In which of the three modes the switched capacitive voltage converter operates is determined by the patterns of switching signals which control the first, the second, the third, the fourth and the fifth switching means.

The switched capacitive voltage converter defined in the opening paragraph is further characterized in that the first, the second, the third, and the fourth switching means are
30 adapted to alternately couple either the first electrode of the first capacitive element to the input terminal and the second electrode of the first capacitive element to the output terminal, or the first electrode of the first capacitive element to the output terminal and the second electrode of the first capacitive element to the reference terminal. Thus, its achieved that the switched capacitive voltage converter is in the down conversion mode.

The switched capacitive voltage converter defined in the opening paragraph is further characterized in that the first, the second, the fourth and the fifth switching means are adapted to alternately couple either the first electrode of the first capacitive element to the input terminal and the second electrode of the first capacitive element to the reference terminal, or the first electrode of the first capacitive element to the output terminal and the second electrode of the first capacitive element to the input terminal. Thus, it is achieved that the switched capacitive voltage converter is in the up conversion mode.

The switched capacitive voltage converter defined in the opening paragraph is further characterized in that the first and the second switching means are adapted to couple the input terminal to the output terminal. Thus, it is achieved that the switched capacitive voltage converter is in the buffer mode.

The patterns of switching signals can be fixed so as to achieve that the switched capacitive voltage converter is always in the same mode, for example up conversion. However, it is also possible to make the mode dependent on the values of the input voltage and of the desired output voltage, respectively. In this way, it is also possible to make the output voltage adjustable, the desired mode being set automatically.

The switched capacitive voltage converter defined in the opening paragraph is further characterized in that at least one of the first, the second, the third, the fourth and the fifth switching means is realized by means of a DMOS transistor. The afore-mentioned switching means in a switched capacitive voltage converter in accordance with the invention can be equipped with various types of switches, for example, they can also be realized by means of transistors. If the switching means employ DMOS transistors (Double diffused MOS transistors) this has the advantage that the switching losses are lower because the DMOS transistors have a low forward resistance. Another reason for the use of DMOS transistors is that they can handle high voltages and large currents.

DMOS transistors have an intrinsic diode in anti-parallel with their drain-source channel. In some situations the intrinsic diode may become undesirably conductive as a result of which the switched capacitive voltage converter will not function in an optimum manner. In order to avoid this risk, the switched capacitive voltage converter defined in the opening paragraph can further be characterized in that at least one of the first, the second, the third, the fourth and the fifth switching means is realized by means of a DMOS transistor coupled in anti-series.

The invention will be described in more detail with reference to the accompanying drawings, in which:

Figure 1 shows an electrical circuit diagram of an embodiment of a switched capacitive voltage converter in accordance with the invention ;

5 Figure 2 shows the electrical circuit diagram of the embodiment of the switched capacitive voltage converter of Figure 1, to clarify the operation of the switched capacitive voltage converter when it is in the down conversion mode;

 Figure 3 shows the electrical circuit diagram of the embodiment of the switched capacitive voltage converter of Figure 1, to clarify the operation of the switched capacitive
10 voltage converter when it is in the up conversion mode;

 Figure 4 shows the electrical circuit diagram of the embodiment of the switched capacitive voltage converter of Figure 1, to clarify the operation of the switched capacitive voltage converter when it is in the buffer mode; and

 Figure 5 shows a specific form of a switched capacitive voltage converter in
15 accordance with the invention.

In these Figures parts or elements having a like function or purpose bear the same reference symbols.

20 Figure 1 shows an electrical circuit diagram of an embodiment of a switched capacitive voltage converter (hereinafter referred to as voltage converter) in accordance with the invention. The voltage converter has an input terminal I and a reference terminal RF for receiving an input voltage U_i . The voltage converter converts the input voltage U_i , which is supplied by a voltage source VS, into an output voltage U_o between an output terminal O and
25 the reference terminal RF. The voltage converter further comprises first to fifth switching means having first to fifth switches S_1 - S_5 . The voltage converter further includes a first capacitive element, i.e. a first capacitor C_1 , and a second capacitive element; i.e. a second capacitor C_2 . The first switch S_1 has one end connected to the input terminal I and its other end to a first electrode of the first capacitor C_1 . The second switch S_2 has one end connected to the
30 first electrode of the first capacitor C_1 and its other end to the output terminal O. The third switch S_3 has one end connected to the second electrode of the first capacitor C_1 and the output terminal O. The fifth switch S_5 has one end connected to the input terminal I and its other end to the second electrode of the first capacitor C_1 . The fourth switch S_4 is connected between the second electrode of the first capacitor C_1 and the reference terminal RF. The second capacitor

C_2 is connected between the output terminal O and the reference terminal RF. Each of the switches S_1 - C_5 can be in a permanently open or closed state or in a periodically alternating open and closed state. Thus, the voltage converter has three possible modes, namely an up conversion mode, a down conversion mode or a buffer mode.

Figure 2 shows the situation in which the voltage converter is in the down conversion mode. In this mode the first to the fourth switch S_1 - S_4 are alternately opened and closed periodically and the fifth switch S_5 is permanently open. The first and the third switch S_1 , S_3 are opened and closed in phase with one another (which is indicated by the reference symbol "f"), while the second and the fourth switch S_2 , S_4 are opened and closed in phase opposition to one another (which is indicated by the reference symbol " f_b "). The output voltage U_0 can be calculated by means of formula [1]:

$$U_0 = \{2 \cdot C_1 \cdot C_2 / (C_1 + C_2)^2\} \cdot U_i \quad [1]$$

In formula [1] C_1 and C_2 represent the capacitance values of the first capacitor C_1 and the second capacitor C_2 . The output voltage U_0 is at the most equal to half the input voltage U_i .

This is reached when the capacitance value C_1 is equal to the capacitance value C_2 .

Figure 3 shows the situation in which the voltage converter is in the up conversion mode. In this mode the first, the second, the fourth and the fifth switch S_1 , S_2 , S_4 , S_5 are alternately closed and opened periodically and the third switch S_3 is permanently open. The second and the fifth switch S_2 , S_5 are opened and closed in phase with one another (which is indicated by the reference symbol "f"), while the second and the fourth switch S_2 , S_4 are opened and closed in phase opposition (which is indicated by the reference symbol " f_b ") with respect to the second and the fifth switch S_2 , S_5 . The output voltage U_0 is (approximately) twice as high as the input voltage U_i .

Figure 4 shows the situation in which the voltage converter is in the buffer mode. In this mode the first and the second switch S_1 , S_2 are permanently closed and the third and the fifth switch S_3 , S_5 are permanently open. Whether the fourth switch S_4 is permanently closed, permanently open, or is alternately opened and closed periodically is in principle irrelevant, in all the cases the voltage converter is in the buffer mode and the output voltage U_0 is (substantially) equal to the input voltage U_i . However, it is advisable to keep the fourth switch S_4 permanently closed. In that case the first and the second capacitor C_1 , C_2 are arranged in parallel and together form a smoothing capacitance for the output voltage U_0 .

Figure 5 shows a specific form of the voltage converter in accordance with the invention. The first to the fifth switch S_1 to S_5 are formed by means of DMOS transistors. In order to prevent undesired conduction of the intrinsic diodes of the DMOS transistors one or

more of the switches S_1 to S_5 can be realized by means of DMOS transistors coupled in ant-series. In Figure 5 this has been done, by way of example, for the first and the second switch S_1 , S_2 .

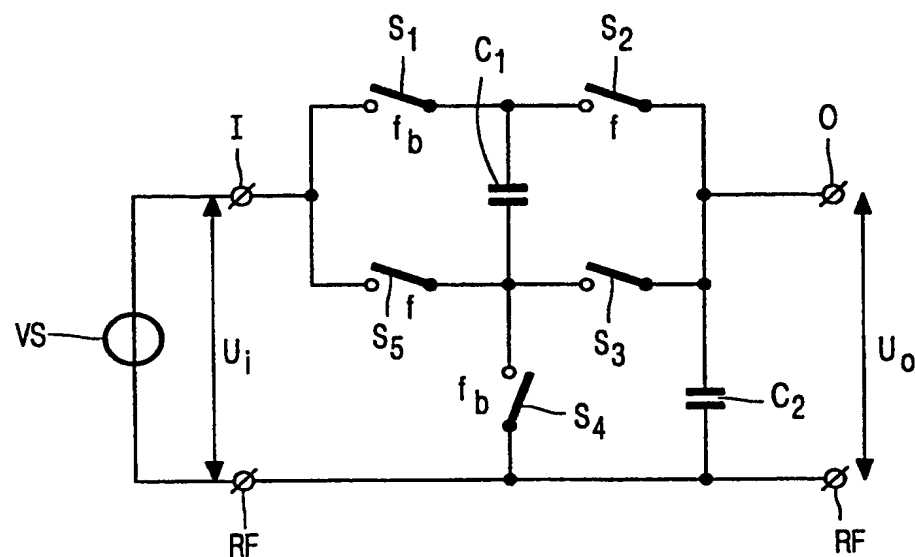
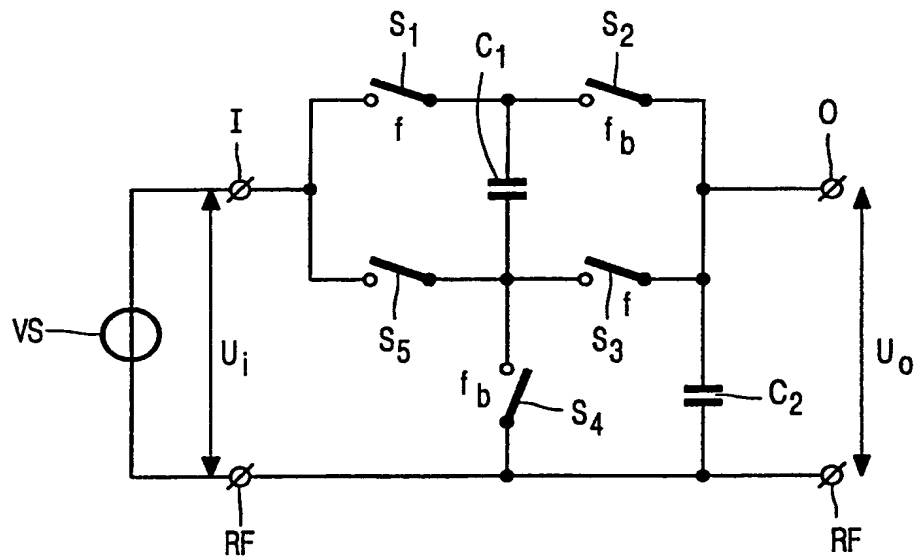
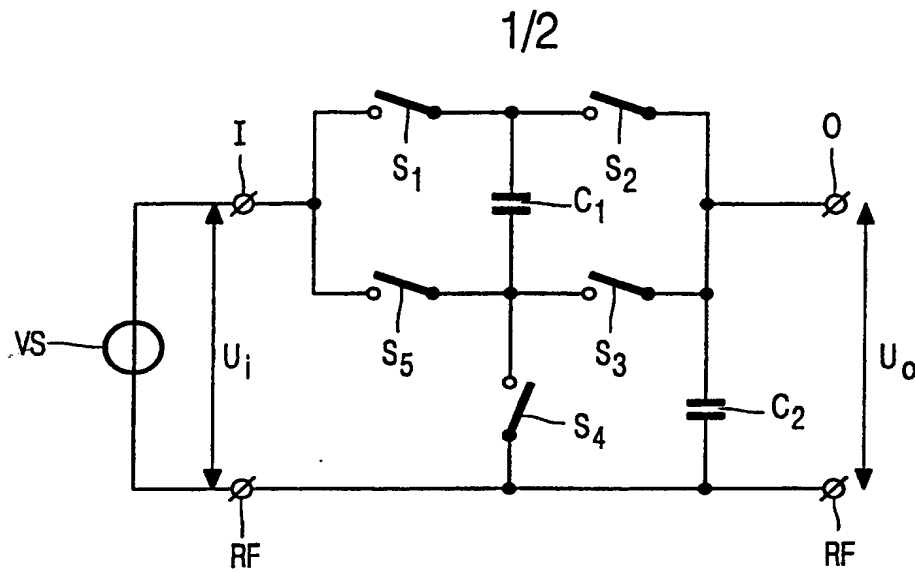
5 For the first to the fifth switch S_1 to S_5 various electronic components such as relays, diodes, transistors and thyristors can be used. The voltage converter in accordance with the invention can be realized as an integrated circuit but also by means of discrete components.

CLAIMS:

1. A switched capacitive voltage converter for converting an input voltage (U_i) between an input terminal (I) and reference terminal (RF) to an output voltage (U_o) between an output terminal (O) and the reference terminal (RF), characterized in that the switched capacitive voltage converter comprises: a first capacitive element (C_1); a second capacitive element (C_2) coupled between the output terminal (O) and the reference terminal (RF); first switching means (S_1) coupled between the input terminal (I) and a first electrode of the first capacitive element (C_1); second switching means (S_2) coupled between the output terminal (O) and the first electrode of the first capacitive element (C_1); third switching means (S_3) coupled between the output terminal (O) and a second electrode of the first capacitive element (C_1); first switching means (S_4) coupled between the first electrode of the first capacitive element (C_1) and the reference terminal (RF); and fifth switching means (S_5) coupled between the input terminal (I) and the second electrode of the first capacitive element (C_1).
2. A switched capacitive voltage converter as claimed in Claim 1, characterized in that the first (S_1), the second (S_2), the third (S_3), and the fourth (S_4) switching means are adapted to alternately couple either the first electrode of the first capacitive element (C_1) to the input terminal (I) and the second electrode of the first capacitive element (C_1) to the output terminal (O), or the first electrode of the first capacitive element (C_1) to the output terminal (O) and the second electrode of the first capacitive element (C_1) to the reference terminal (RF).
3. A switched capacitive voltage converter as claimed in Claim 1, characterized in that the first (S_1), the second (S_2), the fourth (S_4) and the fifth (S_5) switching means are adapted to alternately couple either the first electrode of the first capacitive element (C_1) to the input terminal (I) and the second electrode of the first capacitive element (C_1) to the reference terminal (RF), or the first electrode of the first capacitive element (C_1) to the output terminal (O) and the second electrode of the first capacitive element (C_1) to the input terminal (I).
4. A switched capacitive voltage converter as claimed in Claim 1, characterized in that the first (S_1) and the second (S_2) switching means are adapted to couple the input terminal (I) to the output terminal (O).

5. A switched capacitive voltage converter as claimed in Claim 1, characterized in that at least one of the first (S_1), the second (S_2), the third (S_3), the fourth (S_4) and the fifth (C_5) switching means is realized by means of a DMOS transistor.

6. A switched capacitive voltage converter as claimed in Claim 1, characterized in
5 that at least one of the first (S_1), the second (S_2), the third (S_3), the fourth (S_4) and the fifth (C_5) switching means is realized by means of a DMOS transistor coupled in anti-series.



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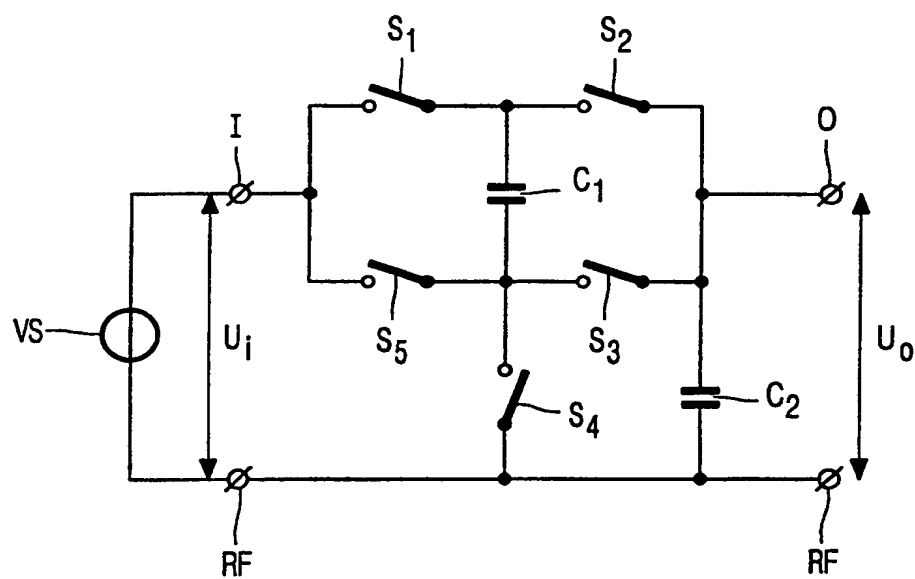


FIG. 4

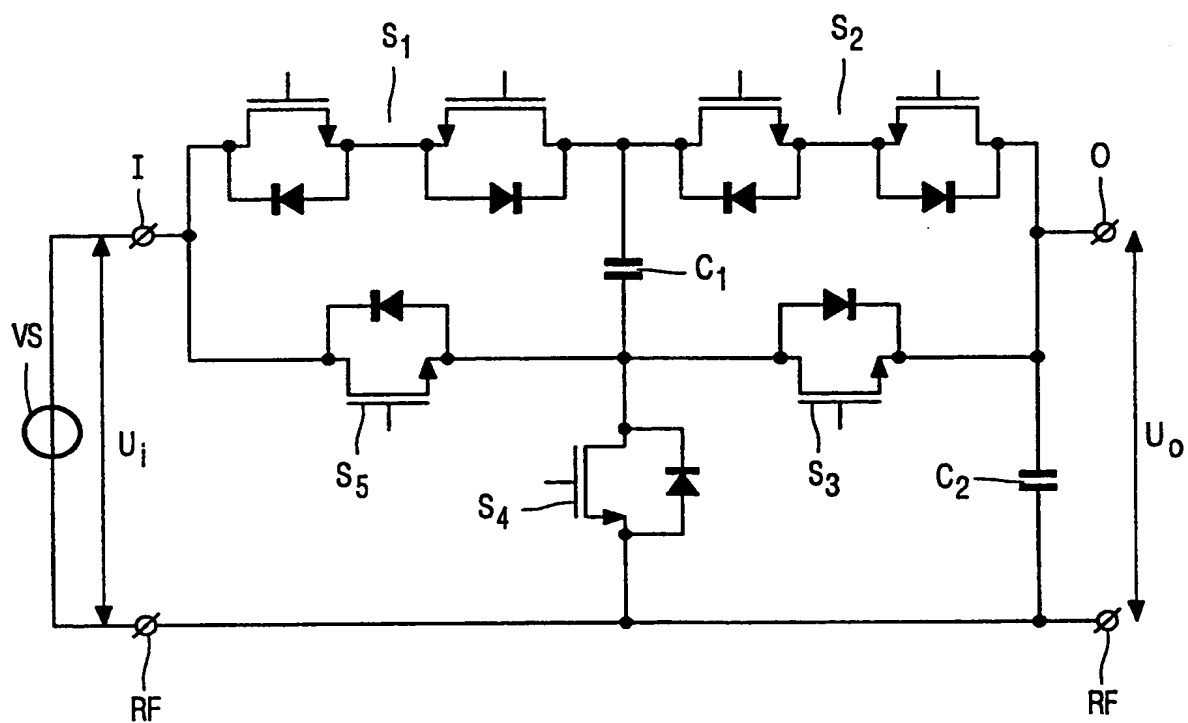


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.

PCT/IB 99/00628

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H02M 3/07

According to International Patent Classification (IPC) or to both national classification and IPC

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5581454 A (HANSEL COLLINS), 3 December 1996 (03.12.96), column 7, line 7 - line 20, figure 3 --	1-6
A	EP 0376627 A2 (MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.), 4 July 1990 (04.07.90), page 5, line 12 - line 28, figure 1 --	1-6
A	EP 0547803 A2 (NOKIA MOBILE PHONES LTD.), 23 June 1993 (23.06.93), figure 2, abstract --	1-6

☒ Further documents are listed in the continuation of Box C.☒ See patent family annex.

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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5680300 A (THOMAS S. SZEPESE ET AL.), 21 October 1997 (21.10.97), figure 2, abstract -- -----	1-6

INTERNATIONAL SEARCH REPORT

Information on patent family members

30/08/99

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Patent document cited in search report			Publication date	Patent family member(s)	Publication date
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EP	0376627	A2	04/07/90	DE 68921322 D,T JP 2276466 A	21/09/95 13/11/90
EP	0547803	A2	23/06/93	DE 69224602 D FI 90606 B,C FI 916007 A JP 6014530 A	00/00/00 15/11/93 20/06/93 21/01/94
US	5680300	A	21/10/97	AU 1523197 A WO 9723944 A	17/07/97 03/07/97

